IN THE CLAIMS

1. (currently amended) A message writing apparatus characterized by comprising:

receiving means (21b) for receiving cells having path information, said cells being obtained by division of a variable-length message;

message area allocating means (21e) for extracting said path information from the received cells received by said receiving means (21b) to allocate a memory area (22) corresponding to said path information, said memory area (22) being larger than a size of said variable-length message;

writing ranking adding means [[(23)]] (21c) for adding writing ranks to the received cells when the received cells are written in said memory area (22) allocated by said message area allocating means (21e); and

storing means (25) for writing the received cells in said memory area (22) according to said writing ranks added by said writing rank adding means [[(23)]] (21c).

2. (original) A message writing apparatus according to claim 1, characterized in that said message area allocating means (21e) includes:

address table setting means for setting, in said memory area (22), an address table area (23) in which a size of a writing area, a writing position of said variable-length message and the number of received cells, corresponding to said path information, are related to each other on the basis of cell numbers and message number of the received cells; and

message storing area setting means for setting, in said memory area (22), a message storing area (24) which CPU reads out the received cells in message units.

3. (currently amended) A message writing apparatus according to claim 1, characterized in that said writing rank adding means [[(23)]] (21c) is made to add said writing ranks to said received cells in the order of receiving processing of the received cells.

4. (currently amended) A message writing apparatus according to claim 1, characterized in that said writing rank adding means [[(23)]] (21c) is made to add said writing ranks to said received cells by writing flag information indicative of whether or not the received cells are read out, in flag areas (K1, ···, Ka) placed in said memory area (22).

5. (currently amended) A message writing apparatus according to claim 4, characterized in that said writing rank adding means [[(23)]] (21c) is equipped with residual quantity examining means ($K_{2\text{-}1}$, ···, $K_{2\text{-}n}$) for checking said flag information to examine a size of a free area for writing of the received cells.

6. (currently amended) A message writing apparatus according to claim 1, characterized in that said writing rank adding means [[(23)]] (21c) is made to add said writing ranks by reading out an indication of a head address holding section (40a, 40b) which manages writing positions for writing of the received cells in said memory area (22) and an indication of a message storing/holding section (41a, 41b, 41c) which manages a message number of the written received cells and writing position information.

7. (currently amended) A message writing apparatus according to claim 6, characterized in that said writing rank adding means [[(23)]] (21c) is equipped with residual quantity checking

means ($K_{2\text{-}1}$, ···, $K_{2\text{-}n}$) for examining a size of a free area for writing of the received cells by checking the indication of said head address holding section (40a, 40b) and the indication of said message storing/holding section (41a, 41b, 41c).

8. (currently amended) A message writing apparatus according to claim 1, characterized in that said message is an adaptation layer message and said cells are obtained by division of [[sad]] said adaptation layer message.

9. (original) A message writing apparatus according to claim 8, characterized in that said adaptation layer is based on AAL5.

10. (original) A message writing method characterized by comprising:

a receiving step of receiving cells having path information, said cells being obtained by division of a variable-length message;

a message area allocating step of extracting said path information from the received cells received in said receiving step to allocate a memory area (22) corresponding to said path information, said memory area (22) being larger than a size of said variable-length message;

a writing rank adding step of adding writing ranks to the received cells when the received cells are written in said memory area (22) allocated in said message area allocating step; and

a storing step of writing the received cells in said memory area (22) according to said writing ranks added in said writing rank step.

11. (currently amended) A message readout apparatus (20) which reads out each of a plurality of cells constituting a message and written in a memory area (22), characterized by comprising:

first means (22, 25) for reading out said message in accordance with writing ranks added in the order of receive processing of said cells;

second means (22, 25) for reading out said message on the basis of the added writing ranks in a manner that flag information, indicative of whether or not said cells are read out, is written in said memory area (22);

third means (22, 25) for reading out said message on the basis of said writing ranks based on an indication of a message storing/holding section (41a, 41b, 41c) which manages a message number of the received cells written in said memory area and writing position information thereon; and

control means (23) operable [[of]] <u>for</u> selecting any one of said first means (22, 25), said second means (22, 25) and said third means (22, 25) by setting of said memory area (22).

12. (original) A message readout apparatus according to claim 11, characterized in that said message is an adaptation layer message and said cells, said cells being obtained by division of said adaptation layer message.

13. (original) A message readout apparatus according to claim 12, characterized in that said adaptation layer is based on AAL5.

14. (currently amended) A message readout method of reading out each of a plurality of cells constituting a message and written in a memory area (22), characterized by comprising:

a first step of reading out said message in accordance with writing ranks added in the order of receive processing of said cells;

a second step of reading out said message on the basis of the added writing ranks in a manner that flag information, indicative of whether or not the cells are read out, is written in said memory area (22); and

a third step of reading out said message in accordance with said writing ranks provided by an indication of a message storing/holding section (41a, 41b, 41c) which manages a message number of the received cells written in said memory area (22) and writing position information,

with [[any]] one of said first [[means]] step, said second [[means]] step and said third [[means]] step being selectively implemented according to setting of said memory area (22).

15. (currently amended) A memory address control circuit for writing of a variable-length message, characterized by comprising:

a path recognizing section (21a) for receiving cells, said cells being obtained by division said variable-length message and transmitted to extract path information from the received cells;

a receive control section (21c) operable [[of]] for adding writing ranks on writing in a memory (22) in correspondence with said path information outputted from said path recognizing section (21a) and [[of]] for outputting a size of a writing area, a writing position of said variable-length message, and the number of received cells as management information;

a received message assembling section (21b) having an address table (23), in which said size of said writing area, said writing position of said variable-length message, and the number of

received cells, corresponding to said path information, are related to each other on the basis of said management information from said receive control section and operable [[of]] for assembling the received cells with respect to one variable-length message and outputting second write information; and

a memory control section (21e) operable [[of]] for controlling writing in said memory (22) on the basis of said management information from said received message assembling section (21b) and the second write information from the receive control section (21c).

16. (currently amended) A memory address control circuit for readout of a variable-length message, characterized by comprising:

a path recognizing section (21a) for receiving cells, said cells being obtained by division of said variable-length message and transmitted to extract path information from the received cells;

a receive control section (21c) operable [[of]] for adding writing ranks on readout from a memory (22) in correspondence with said path information outputted from said path recognizing section (21a) and [[of]] for outputting a size of a readout area, a readout position of said variable-length message, and the number of received cells as management information;

a received message assembling section (21b) having an address table (23), in which said size of said readout area, said readout position of said variable-length message and the number of received cells being corresponding to said path information, are related to each other on the basis of said management information from said receive control section (21c) and operable [[of]] for assembling the received cells with respect to one variable-length message to output and outputting second readout information; and

a memory control section (21e) operable [[of]] <u>for</u> controlling the readout to said memory (22) on the basis of said management information from said received message assembling section (21b) and said second readout information from said receive control section.